SD8006

4 Diff Channels SD ADC SOC with RTC and 24*8 LCD

Features

- High precision 24 bits ADC, 20 bits effective resolution, 4 differential or 8 single-ended inputs
- Low noise, high input impedance preamplifier with selectable gain: 1, 12.5, 50, 100, or 200; 40nVrms equivalent input noise, 16 bits noise free at ±4mV FSR
- 8 bits RISC ultra low power MCU. Consumes 300uA typically at 2MHz operating clock rate and 3V. Standby current is 1.5uA at 32kHz clock, and less than 1uA at sleep
- Strong anti-interference capability, exceeds 4kV EFT test
- 16K Bytes OTP, 512 Bytes SRAM
- Low OTP programming voltage, can replace external EEPROM
- Multiple clock sources, flexible clock selection, external oscillator malfunction detection
- ADC output rate: 8SPS–2kSPS
- 24SEG X 8COM or 28SEG X 4COM LCD drive, programmable boost module to maintain luminance at low supply voltage
- Built-in temperature sensor, supports single point calibration
- 1.2V low temperature drift voltage reference output
- Selectable voltage source: 2.4V/2.6V/2.9V/3.3V
- Flexible battery voltage detection range 2.0V~ 3.3V
- External or internal voltage reference for ADC, multiple internal voltage references
- RTC module calculates calendar/time information
- Abundant peripheral resources: UART, PDM, PFD, CAPTURE, TIMER, infrared carrier
- Low voltage detection and power on reset circuit
- Operating voltage range: 2.4V~ 3.6V
- Operating temperature range: -40℃~ 85℃

Description

The SD8006 is a CMOS SOC with built-in 24 bit ADC. It has very rich peripheral resources: RTC, UART, selectable voltage source to provide a stable excitation for external transducer, PGIA, voltage step-up module, timer with CAPTURE function, PDM/PFD output, and LCD driver.

Programming voltage for the 16K internal OTP is only 2.4V~3.6V. It can be programmed online and be used in place of external EEPROM.

The IC was designed with ultra low power technology. Typical total operating current is only 750uA.

Three working modes are provided so users can select the optimum choice between speed and power. They are normal mode, standby mode, and sleep mode.

The IC has strong anti-interference capability. It passes 4kV Electrical Fast Transient (EFT) test easily without using any additional protective circuit, and is suitable for harsh environment applications.

If external oscillator is used but stopped due to some interference, the internal 4MHz RC oscillator is waken up immediately. Its frequency is halved and becomes the new clock source. An interrupt is generated and the IC functions continuously.

Applications

Health scale, jewelry scale, bridge type weak signal transducer signal processing applications

Ordering Information

Bare die or custom made PCB module

Pin Diagram and Descriptions

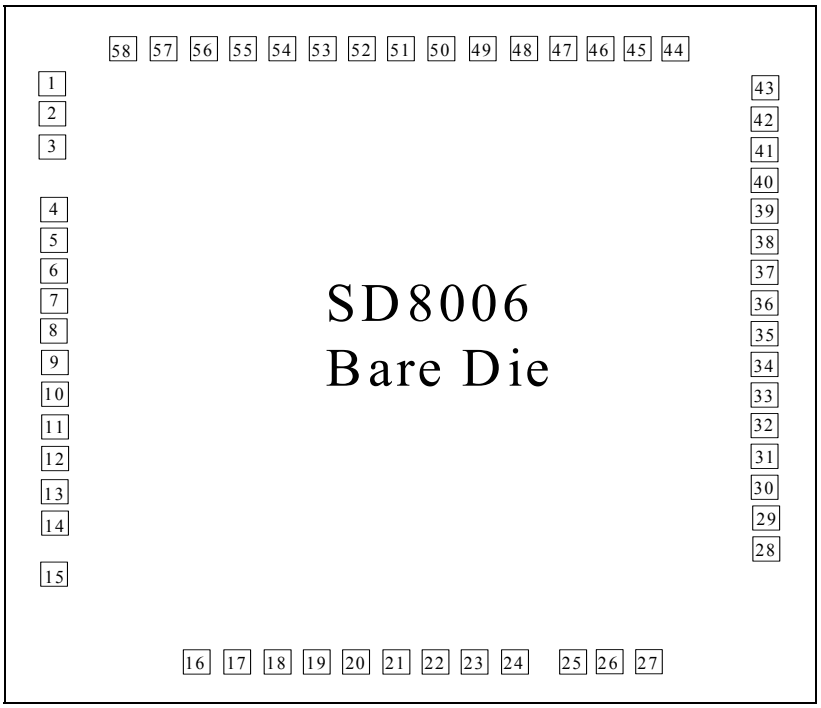

Figure 1. Pad diagram

Table 1. Pad Descriptions

Pad No.	Pin Name	Attribute	Description
1-2	CP, CN	Analog	External capacitor connection pins for the voltage booster circuit. Capacitor not needed if high frequency RC clock is used for the booster
3	VLCD	Analog	LCD driver power supply, internally connect to DVDD or booster output through register setting, connect 1uF filter capacitor to DVDD
4	ACM	Analog	1.2V reference output, floating when ACM is shutdown, connect 0.1uF cap to AVSS
5-12	AI0--AI7	Analog input	Analog signal inputs, each port has an independent register controlled pull-down resistor (default OFF), should set to ON for unused port; AI0-AI1, AI2-AI3, AI4-AI5, AI6-AI7 can be used as 4 differential or 8 single-ended inputs
13	AVDDR	Analog	Internal LDO output for IC's analog module, can provide excitation to external transducer, connect 0.1uF to 10uF filter capacitor to AVSS
14	AVDD	Power	Analog supply voltage, connect 0.1uF capacitor to AVSS
15	AVSS	Ground	Analog ground
16-20	P00/KEY0 -- P04/KEY4	I/O	Digital port P00-04 or external key inputs KEY0-4
21	P05/LBTIN	I/O	Digital port P05 or low battery detect LBTIN input
22-23	P06/XOUT -- P07/XIN	Analog , I/O	Digital ports P06-P07, or 32.768kHz or 1MHz-4MHz crystal oscillator pins XIN can be used as external clock input
24	DVDD	Power	Digital supply voltage, connect 1uF capacitor to DVSS
25	DVSS	Ground	Digital ground
26	VPP	I	OTP high voltage programming pin, connect 1uF capacitor to DVDD or DVSS
27	P27/SEG27/BUZ	I/O	Digital port P27, LCD segment SEG27, or Buzzer BUZ output
28	P26/SEG26	I/O	Digital port P26 or LCD segment SEG26
29	P25/SEG25/T0CK	I/O	Digital port P25, LCD segment SEG25, or TIMER0 external clock T0CK input
30	P24/SEG24/ PFD	I/O	Digital port P24, LCD segment SEG24, or Programmable frequency divider PFD
31-32	P23/SEG23-- P22/SEG22	I/O	Digital port P23-22 or LCD segment SEG23-22
33	P21/SEG21/INT1	I/O	Digital port P21, LCD segment SEG21, or External interrupt INT1
34	P20/SEG20/INT0	I/O	Digital port P20, LCD segment SEG20, or External interrupt INT0
35-36	P57/SEG19/ TXD-- P56/SEG18/ RXD	I/O	Digital port P57-56, LCD segment SEG19-18, or UART data transmit TXD and data receive RXD
37	P55/SEG17/ PWM/PDM	I/O	Digital port P55, LCD segment SEG17, or PWM0/PDM0 output
38	P54/SEG16/ CLKout	I/O	Digital port P54, LCD segment SEG16, or selectable clock output CLKout
39	P53/SEG15/CCP	I/O	Digital port P53, LCD segment SEG15, or compare/capture output CCP0
40-50	P52/SEG14 -- P40/SEG4	I/O	Digital port P52-50/P47-40 or LCD SEG14-4
51-58	P37/COM7/ -- P30/COM0	I/O	Digital port P37-30 or LCD COM7-0 At 4COM mode, COM7-4 are used as SEG3-0 During serial programming, COM3-0 serve as Data Output, 2MHz clock Input, Data Input, and Data Clock

Remark:

1. All I/O ports Pnn have internal pull-up option (default OFF) and input hysteresis at 0.3VDD/0.7VDD.
2. Product improvements that do not affect the functions described in this data sheet may be made without notice.

Functional Block

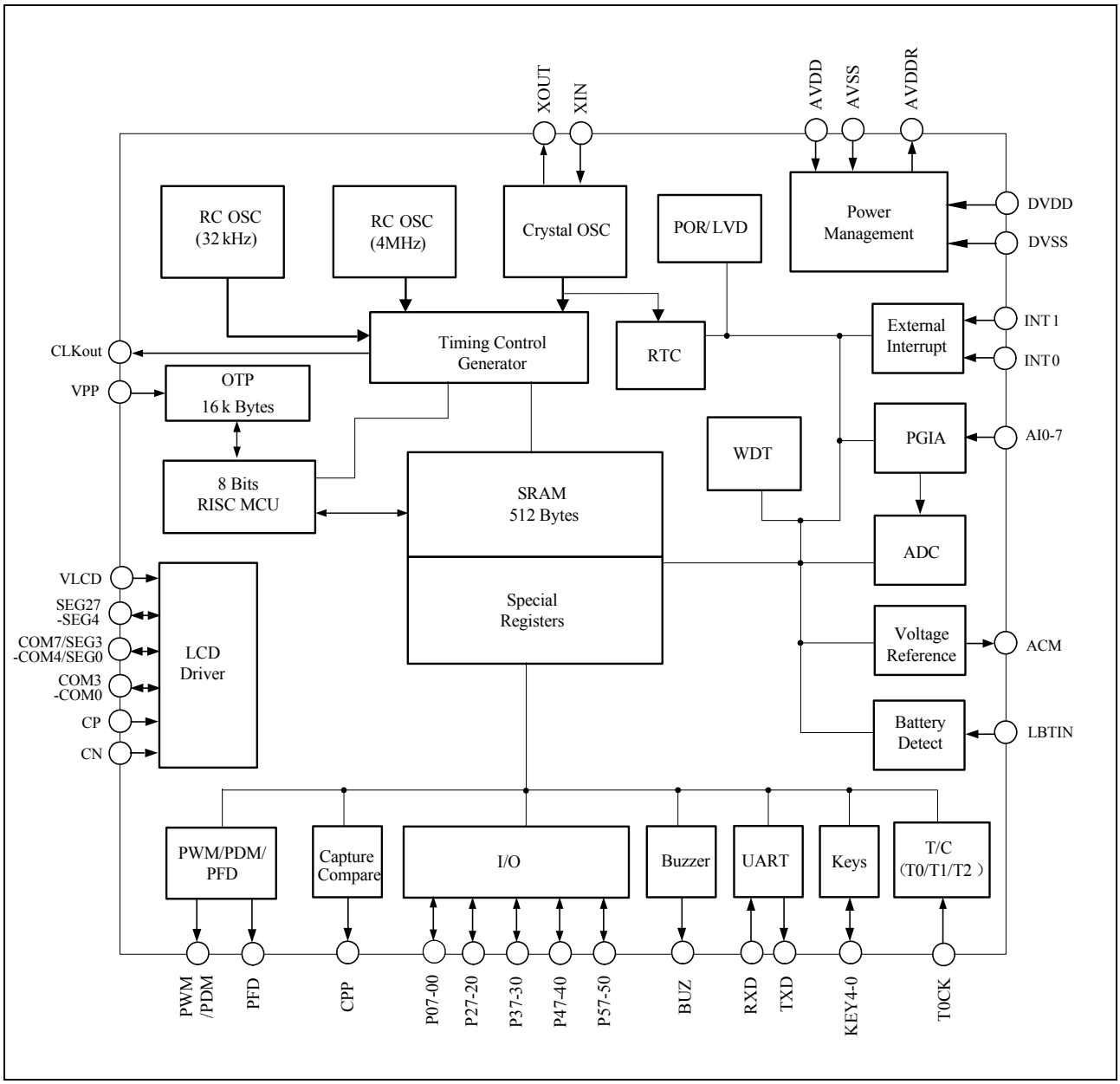

Figure 2. Functional block diagram

Typical Applications

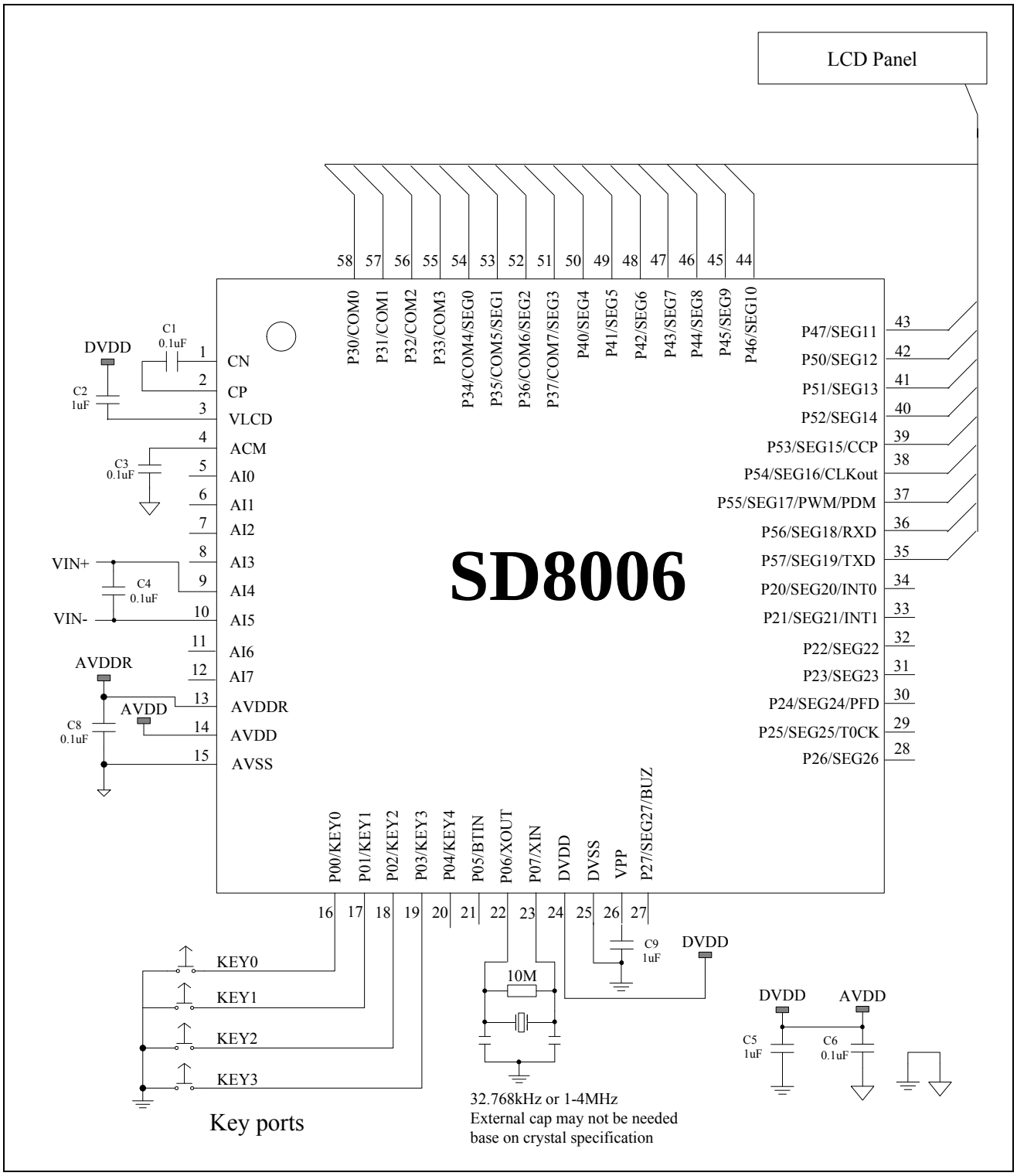

Figure 3. Typical application diagram

Electrical Specifications

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-40	+85	°C
T_S	Storage temperature	-55	+150	°C
V_{DD}	Supply voltage	-0.2	+4.0	V
Vpp	Programming voltage	-0.2	+7.5	V
V_{IN}, V_{OUT}	Digital input/output voltage	-0.2	V_{DD}+0.3	V
T_L	Reflow temperature profile	Per IPC/JEDECJ-STD-020C		°C

Remarks:

1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and careful not to exceed the operating voltage range.
2. Turn off power before insert or remove the device.

Table 3. Electrical Specifications（VDD=3V, T_A=25℃）

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
VDD	Supply voltage	2.4	3.0	3.6	V	Analog modules operating voltage
		2.0	3.0	3.6	V	Digital modules and MCU operating voltage
FOSC	Operating frequency	16k	2M	4M	Hz	FOSC must be 2MHz when read/write tables in OTP
IHRC	Internal high frequency RC oscillator	--	4	--	MHz	
ILRC	Internal low frequency RC oscillator	28	--	36	kHz	
HXT	External high frequency crystal oscillator	1	--	6	MHz	
LXT	External low frequency crystal oscillator	16	32.786	--	kHz	
IDD1	Operating current 1	--	750	--	uA	4MHz ext crystal freq halved for MCU Analog modules active
		--	720	--		4MHz internal RC oscillator freq halved for MCU Analog modules active
IDD2	Operating current 2	--	330	--	uA	4MHz external crystal freq halved for MCU Analog modules inactive
		--	300	--		4MHz internal RC oscillator freq halved for MCU Analog modules inactive
IDD3	Operating current 3	--	8	--	uA	32.768kHz external crystal for MCU Analog modules inactive
		--	6	--	uA	32kHz internal RC oscillator for MCU Analog modules inactive
IDD4	Operating current 4	--	4	--	uA	32.768kHz external crystal for MCU MCU at standby mode Analog modules inactive
		--	1.5	--		32kHz internal RC oscillator for MCU MCU at standby mode Analog modules inactive
IDD5	Operating current 5	--	0.2	1	uA	MCU at sleep mode Analog modules inactive

Fsam	ADC sampling rate	--	128	--	kHz	
OSR	Over sampling rate	128	--	65536		
NFbit	Noise free bits[1]	--	16	--	bits	Gain=200, input FSR=±4mV
NMbit	No missing code	--	--	24	bits	
INL	INL	--	0.002	--	%FSR	
VINdif	PGIA differential input range	--	--	1800	mV	1X gain
		-Vref/12.5	--	Vref/12.5		12.5X gain
		-Vref/50	--	Vref/50		50X gain
		-Vref/100	--	Vref/100		100 X gain
		-Vref/200	--	Vref/200		200 X gain
VIN	PGIA input voltage range[2]	-0.3	--	AVDDR		1X gain and buffer is off
		0.3	--	AVDDR-0.7		1X gain and buffer is on, or gain≠1
Nrms	RMS noise	--	40	--	nVrms	200X gain
Vacm	ACM voltage output	--	1.2	--	V	
IacmSour	ACM current source	--	1	--	mA	
IacmSink	ACM current sink	--	1	--	mA	
PSRacm	ACM PSR	--	100	--	uV/V	
Tgain	Gain tempco	--	±4	--	ppm/℃	-10℃ to +40℃
Vavddr	AVDDR Voltage output	--	2.4	--	V	AVDDRX [1:0]=00
		--	2.6	--		AVDDRX [1:0]=01
		--	2.9	--		AVDDRX [1:0]=10
		--	3.3	--		AVDDRX [1:0]=11
Iavddr	AVDDR current	--	10	--	mA	
POR	POR voltage	--	2.0	--	V	
LVD	LVD voltage	--	1.9	--	V	
THlbt	LVD hysteresis	--	200	--	mV	
Vlbt	Low VDD alarm threshold	--	3.3	--	V	LBTX[3:0]=0010
		--	3.2	--		LBTX[3:0]=0011
		--	3.1	--		LBTX[3:0]=0100
		--	3.0	--		LBTX[3:0]=0101
		--	2.9	--		LBTX[3:0]=0110
		--	2.8	--		LBTX[3:0]=0111
		--	2.7	--		LBTX[3:0]=1000
		--	2.6	--		LBTX[3:0]=1001
		--	2.5	--		LBTX[3:0]=1010
		--	2.4	--		LBTX[3:0]=1011
		--	2.3	--		LBTX[3:0]=1100
		--	2.2	--		LBTX[3:0]=1101
		--	2.1	--		LBTX[3:0]=1110
		--	2.0	--		LBTX[3:0]=1111
Vlcd	LCD charge pump output voltage	--	2.1	--	V	VLCDX[2:0]=000
		--	2.3	--		VLCDX[2:0]=001
		--	2.5	--		VLCDX[2:0]=010
		--	2.7	--		VLCDX[2:0]=011
			2.9			VLCDX[2:0]=100
		--	3.1	--		VLCDX[2:0]=101
		--	3.3	--		VLCDX[2:0]=110
		--	3.5	--		VLCDX[2:0]=111

Ilcd	LCD charge pump current[3]	--	--	500	uA	
Digital I/O parameter						
IOL	Output low current sink	--	3	--	mA	VOL=0.3V, PTxSR=0
		--	12	--		VOL=0.3V, PTxSR=1
IOH	High output current source	--	3	--	mA	VOH=VDD-0.3V, PTxSR=0
		--	12	--		VOH=VDD-0.3V, PTxSR=1
VIH	Input high voltage	0.7VDD	--	--	V	
VIL	Input low voltage	--	--	0.3VDD	V	
VOH	Output high voltage	VDD-0.3	--	--	V	
VOL	Output low voltage	--	--	VSS+0.3	V	

Note:

1. Noise free bits and effective resolution are both related to the signal's full scale range. Its peak to peak or rms noise plays the decisive role.
2. The signal input range is limited by the differential signal input range and the absolute voltage at the input terminals. The first one is the real signal input range. It is affected by the PGIA gain and the ADC voltage reference choice. The second one includes both differential and common mode components and is mainly limited by the circuit.
3. The charge pump driving capability is related to the choice of capacitor and the operating frequency.