SD8000S

20 bits ADC SOC with RTC

Features

- High precision ADC, 20 bits effective resolution
- Low noise, high input impedance preamplifier with selectable gain: 1, 12.5, 50, 100, or 200
- 8 bits RISC ultra low power MCU, 49 instructions and 6 stack levels. At 2MHz operating clock rate and 3V, current consumption is 300uA typically, 1uA at standby and 32kHz clock, and less than 1uA at sleep
- 16k Bytes OTP, 256 Bytes SRAM
- Low OTP programming voltage
- Internal RC oscillator. Provides second, minute, hour data when 32.768kHz crystal is connected
- 8 bits interrupt timer, supports PFD output
- Built-in temperature sensor, supports single point calibration
- 14SEG X 4COM LCD drive, programmable boost module
- Selectable voltage source: 2.4V/2.6V/2.9V/3.3V
- Flexible battery voltage detection: 2.0V~ 3.3V
- Schmitt trigger input, pull up resistor selectable
- Watch Dog Timer
- Low voltage detection and power on reset circuit
- Operating voltage range: 2.4V~ 3.6V
- Operating temperature range: -40℃~ 85℃

Description

The SD8000S is a CMOS SOC with built-in 20 bits ADC and 16k Bytes OTP memory. The built-in OTP has low programming voltage at 2.4V~ 3.6V. It can be used in place of external EEPROM. The only external components needed for a SD8000S based body weight scale are five capacitors.

The IC was designed with ultra low power technology. Operating at 2MHz operating clock rate and 3V supply, the total typical operating current is 650uA (external transducer driving current not included). Such low current consumption is very suitable for battery powered applications.

Three working modes are provided so users can select the optimum choice between speed and power. They are normal mode, standby mode, and sleep mode.

The LCD driver consumes ultra low power but has high driving capacity. Luminance level is adjustable. The embedded programmable boost module allows brightness to be maintained during low voltage condition.

Selectable voltage source provides a stable excitation to external transducer.

All I/O ports have Schmitt trigger input function. Built-in pull-up resistor option is available at every input port.

Applications

Body weight scale, kitchen scale, palm scale, portable scale

Ordering Information

Bare die or custom made PCB module

Pin Diagram and Descriptions

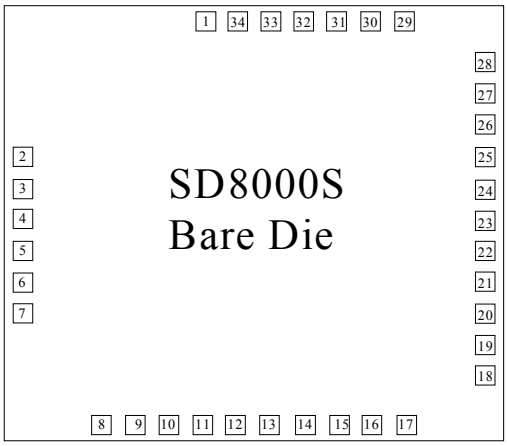

Figure 1. Pad diagram

Table 1. Pad Descriptions

Pad No.	Pin Name	Attribute	Description
1	VLCD	Analog	LCD driver power supply, internally connect to DVDD or booster output through register setting, connect 1uF filter capacitor to DVDD
2	NC	NC	No connect. Must not connect to any circuit
3	AIP	Analog input	Analog signal differential inputs Should enable the internal pull-down resistor for unused input
4	AIN		
5	AVDDR	Analog	Internal LDO output for IC's analog module, can provide excitation to external transducer, connect 0.1uF filter capacitor to AVSS
6	AVDD	Power	Analog supply voltage, connect 0.1uF capacitor to AVSS
7	AVSS	Ground	Analog ground
8	P20/INT0	I/O	Digital port P20 or external interrupt INT0
9	P21/INT1/ PFD	I/O	Digital port P21, external interrupt INT1, or programmable frequency divider PFD output
10	P22/LBTIN	I/O	Digital port P22 or low battery detect LBTIN input
11	P23/BUZ	I/O	Digital port P23 or buzzer BUZ output
12	DVDD	Power	Digital supply voltage, connect 1uF capacitor to DVSS
13	DVSS	Ground	Digital ground
14	VPP	I	OTP high voltage programming pin, connect 1uF capacitor to DVDD or DVSS
15	P24/XIN	I/O	Digital port P24 or 32.768kHz crystal oscillator input XIN
16	P25/XOUT	I/O	Digital port P25 or 32.768kHz crystal oscillator output XOUT
17	P26/PFD/ SEG13	I/O	Digital port P26, PFD output, or LCD SEG13
18	P27 /BUZ/SEG12	I/O	Digital port P27, BUZ output, or LCD SEG12
19-30	P47/SEG11 -- P34/SEG0	I/O	Digital port P47-P40/P37-P34 or LCD SEG11-SEG0
31-34	P33/COM3 -- P30/COM0	I/O	Digital port P33-P30 or LCD COM3-COM0

Remark: All I/O ports Pnn have internal pull-up option (default OFF) and input hysteresis at 0.3VDD/0.7VDD.

Functional Block

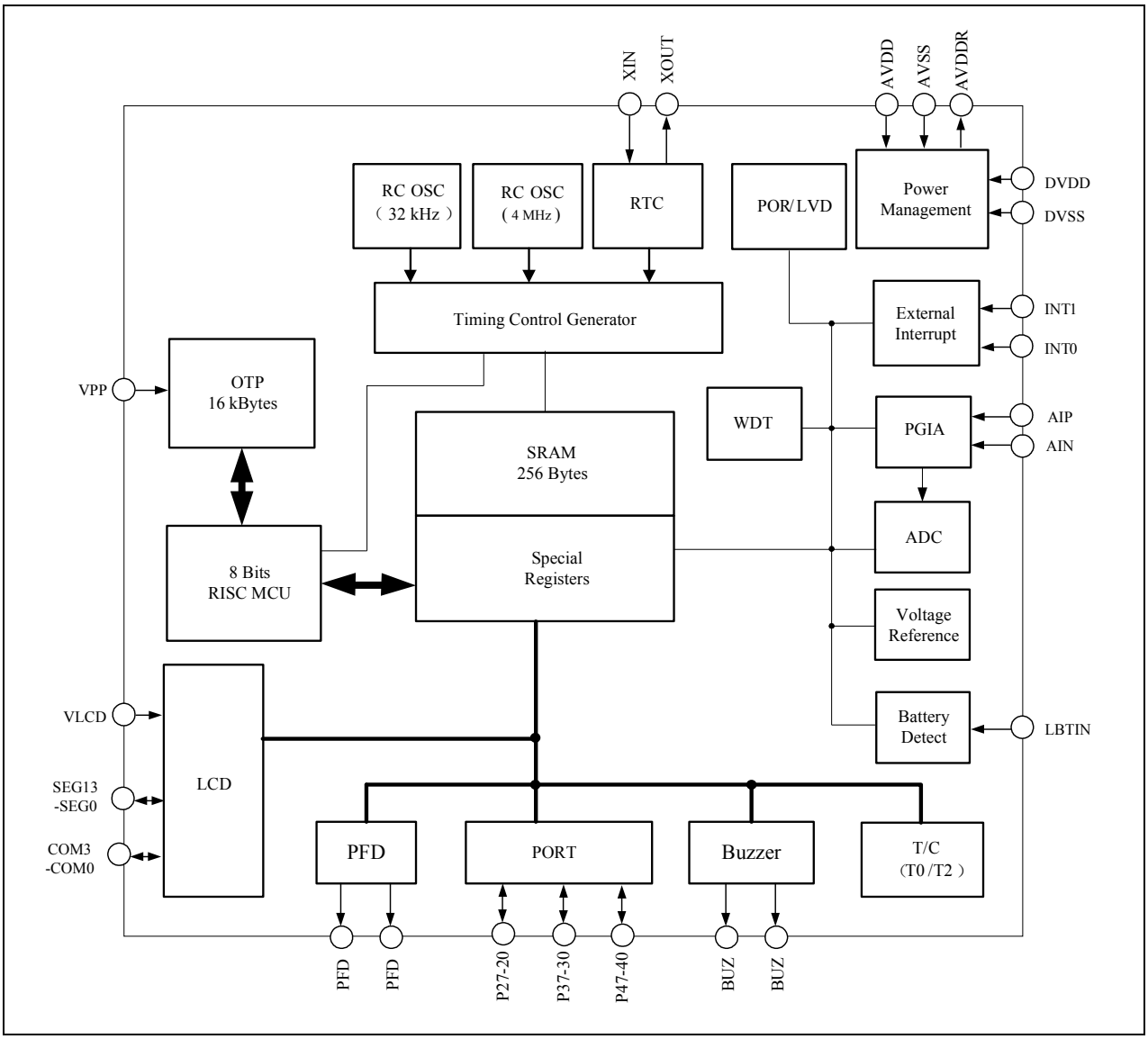

Figure 2. Functional block diagram

Typical Applications

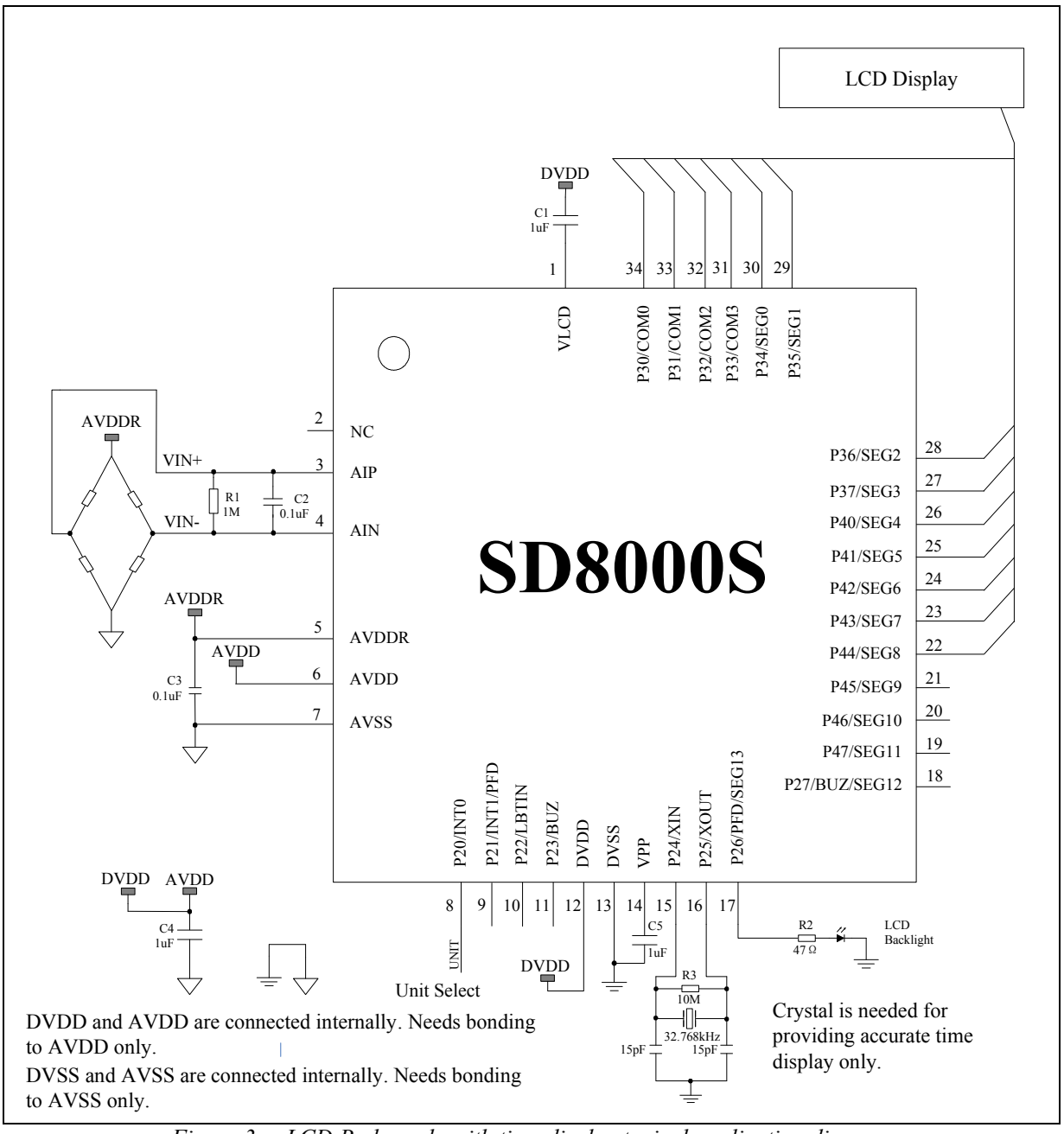

Figure 3. LCD Body scale with time display typical application diagram

Electrical Specifications

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-40	+85	°C
T_S	Storage temperature	-55	+150	°C
V_{DD}	Supply voltage	-0.2	+4.0	V
Vpp	Programming voltage	-0.2	+7.5	V
V_{IN}, V_{OUT}	Digital input/output voltage	-0.2	V_{DD}+0.3	V
T_L	Reflow temperature profile	Per IPC/JEDECJ-STD-020C		°C

Remarks:
1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and careful not to exceed the operating voltage range.
2. Turn off power before insert or remove the device.

Table 3. Electrical Specifications（VDD=3V, T_A=25℃）

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
VDD	Supply voltage	2.4	3.0	3.6	V	Analog modules operating voltage
		2.0	3.0	3.6	V	Digital modules and MCU operating voltage
FOSC	Operating frequency	16k	2M	4M	Hz	FOSC must be 2MHz when read/write tables in OTP
IHRC	Internal high frequency RC oscillator	--	4	--	MHz	Frequency after calibration
ILRC	Internal low frequency RC oscillator	28	--	36	kHz	Frequency after calibration
LXT	External low frequency crystal oscillator	16	32.786	--	kHz	
IDD1	Operating current 1	--	650	--	uA	2MHz internal RC oscillator for MCU Digital and analog modules both active
IDD2	Operating current 2	--	6	--	uA	32kHz internal RC oscillator for MCU Digital module active Analog modules inactive
IDD3	Operating current 3	--	1	--	uA	32kHz internal RC oscillator for MCU MCU at standby mode Analog modules inactive
IDD4	Operating current 4	--	--	1	uA	MCU at sleep mode Analog modules inactive
Fsam	ADC sampling rate	--	--	256	kHz	
OSR	Over sampling rate	128	--	16384		
NFbit	Noise free bits[1]	--	16	--	bits	Gain=200, input FSR=±4mV
VINpga	PGIA differential input range	--	--	1800	mV	1X gain
		-Vref/12.5	--	Vref/12.5		12.5X gain
		-Vref/50	--	Vref/50		50X gain
		-Vref/100	--	Vref/100		100 X gain
		-Vref/200	--	Vref/200		200 X gain

Vavddr	AVDDR Voltage output	--	2.4	--	V	AVDDRX [1:0]=00
		--	2.6	--		AVDDRX [1:0]=01
		--	2.9	--		AVDDRX [1:0]=10
		--	3.3	--		AVDDRX [1:0]=11
Iavddr	AVDDR current	--	10	--	mA	
POR	POR voltage	--	2.0	--	V	
LVD	LVD voltage	--	1.9	--	V	
THlbt	LVD hysteresis	--	200	--	mV	
Vlbt	Low VDD alarm threshold	--	3.3	--	V	LBTX[3:0]=0010
		--	3.2	--		LBTX[3:0]=0011
		--	3.1	--		LBTX[3:0]=0100
		--	3.0	--		LBTX[3:0]=0101
		--	2.9	--		LBTX[3:0]=0110
		--	2.8	--		LBTX[3:0]=0111
		--	2.7	--		LBTX[3:0]=1000
		--	2.6	--		LBTX[3:0]=1001
		--	2.5	--		LBTX[3:0]=1010
		--	2.4	--		LBTX[3:0]=1011
		--	2.3	--		LBTX[3:0]=1100
		--	2.2	--		LBTX[3:0]=1101
		--	2.1	--		LBTX[3:0]=1110
		--	2.0	--		LBTX[3:0]=1111
Vlcd	LCD charge pump output voltage	--	2.1	--	V	VLCDX[2:0]=000
		--	2.3	--		VLCDX[2:0]=001
		--	2.5	--		VLCDX[2:0]=010
		--	2.7	--		VLCDX[2:0]=011
			2.9			VLCDX[2:0]=100
		--	3.1	--		VLCDX[2:0]=101
		--	3.3	--		VLCDX[2:0]=110
		--	3.5	--		VLCDX[2:0]=111
Ilcd	LCD charge pump current[2]	--	--	500	uA	
Digital I/O parameter						
IOL	Output low current sink	--	3	--	mA	VOL=0.3V, PTxSR=0
		--	12	--		VOL=0.3V, PTxSR=1
IOH	High output current source	--	3	--	mA	VOH=VDD-0.3V, PTxSR=0
		--	12	--		VOH=VDD-0.3V, PTxSR=1
VIH	Input high voltage	0.7VDD	--	--	V	
VIL	Input low voltage	--	--	0.3VDD	V	
VOH	Output high voltage	VDD-0.3	--	--	V	
VOL	Output low voltage	--	--	VSS+0.3	V	

Note:

1. Noise free bits and effective resolution are both related to the signal's full scale range. Its peak to peak or rms noise plays the decisive role.
2. The charge pump driving capability is related to the choice of capacitor and the operating frequency.